REMARKS

Applicant is in receipt of the Office Action mailed March 10, 2004.

Art Rejections

Claims 1-4, 6, 8-10, 33-34, and 36-39 were rejected under 35 U.S.C. 102(b) as being anticipated by USPN 5,579,473 to Schlapp et al. (hereinafter referred to simply as Schlapp).

Claim 5 was rejected under 35 U.S.C. 103(a) as being unpatentable over USPN 5,579,473 to Schlapp et al. and USPN 6,415,358 to Arimilli et al.

Claim 7 was rejected under 35 U.S.C. 103(a) as being unpatentable over USPN 5,579,473 to Schlapp et al. and USPN 6,437,789 to Tidwell et al.

Claims 35 and 40 were rejected under 35 U.S.C. 103(a) as being unpatentable over USPN 5,579,473 to Schlapp et al. and USPN 5,787,473 to Vishlitzky et al. (hereinafter referred to simply as Vishlitzky)

Claim 1 as amended recites:

A graphics system comprising:

one or more memories configured to receive and store graphics data, wherein each memory comprises on a single integrated chip,

one or more RAM memories configured to store the graphics data,

a level two cache memory connected to each RAM memory, and

a level one cache memory connected to each of the level two cache memories;

an array of registers configured to store status information, wherein the status information tracks and indicates accesses to the graphics data in the level one cache, wherein the status information further indicates whether the graphics data is modified or unmodified; and

a memory request processor connected to the memories and to the array of registers, wherein the memory request processor is operable to write-back graphics data stored in one of the level one cache memories that the status information indicates is modified to one of the corresponding level two cache memories when an empty memory cycle occurs.

Neither Schlapp nor Vishlitzky, either singly or in combination teach or suggest "a memory request processor connected to the memories and to the array of registers, wherein the memory request processor is operable to write-back graphics data stored in one of the level one cache memories that the status information indicates is modified to one of the corresponding level two cache memories when an empty memory cycle occurs". In fact, Schlapp and Vishlitzky are silent on empty memory cycles.

Therefore, claim 1 is patentably distinguished over Schlapp and/or Vishlitzky.

Claims 33, 40, and new claims 41 and 42 contain limitations similar to claim 1. Thus, claims 1, 33, 40, and 41 and their dependent claims are patentably distinguished over Schlapp and/or Vishlitzky and are allowable for at least the reasons given above in support of claim 1.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert & Goetzel PC Deposit Account No. 50-1505/5181-86900/JCH.

Also enclosed herewith are the following items:

☒ Return Receipt Postcard

☐ Request for Approval of Drawing Changes

☐ Notice of Change of Address

☐ Check in the amount of $ for fees ( ).

☐ Other:

Respectfully submitted,

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AGENT FOR APPLICANT(S)

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